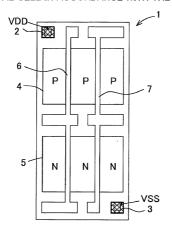
FIG. 1
FUNDAMENTAL CELL IN ACCORDANCE WITH THE PRESENT INVENTION

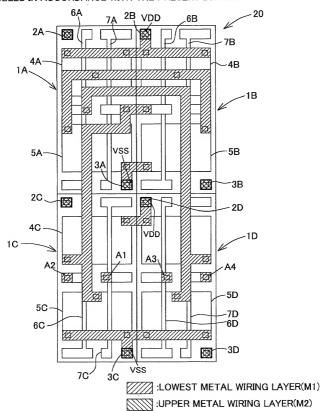


:LOWEST METAL WIRING LAYER(M1)

:UPPER METAL WIRING LAYER(M2)

FIG. 2

FUNCTIONAL CIRCUIT BLOCK FORMED BY USING FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION



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FIG. 3
CIRCUIT DIAGRAM OF THE FUNCTIONAL CIRCUIT BLOCK SHOWN IN FIG.2

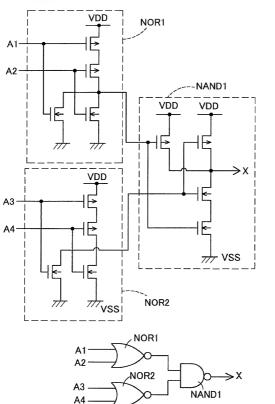


FIG. 4

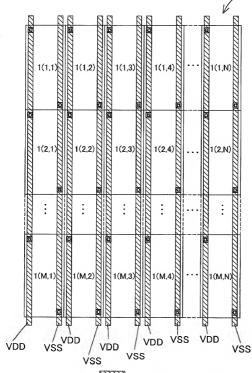
FIRST PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

		/31					
						V	
7	777770	MININI TO THE PARTY OF THE PART	MILLION TO THE	TITINO	777	777770	M VDD
							VUU
	444	4(4.5)	444.5				
	1(1,1)	1(1,2)	1(1,3)	1(1,4)		1(1,N)	
\square							ZZ VSS
		10//////				101////	
							V
	1(2,1)	1(2,2)	1(2,3)	1(2,4)		1(2,N)	
		.,,		, , , ,			
\overline{z}		TTTT VOX	NIIIII NO		777	7777778	⊠ VSS
	:	:	:	:			
\square		TOTAL TOTAL	77777N	7777770	777	70/////00	Z VDD
	1(M,1)	1(M,2)	1(M,3)	1(M,4)		1(M,N)	
i			,-,	, .,		. (,)	
M	AGILLITTI	MEN / / / / /		MITTER TO	,,,,	TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT	⊠ VSS
							V V V

:UPPER METAL WIRING LAYER(M2)

FIG. 5

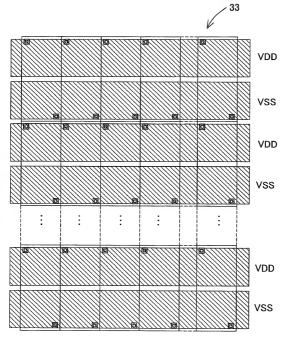
SECOND PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX 232



:UPPER METAL WIRING LAYER(M2)

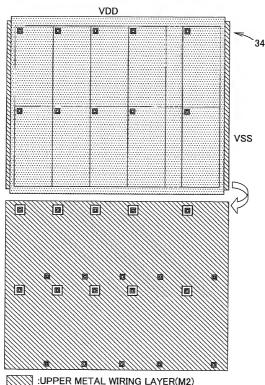
FIG. 6

THIRD PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX





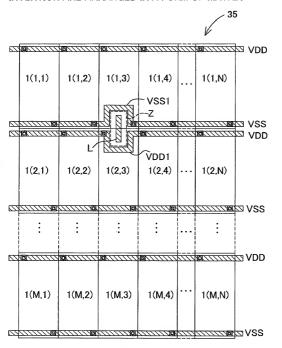
FOURTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX



:UPPER METAL WIRING LAYER(M2)

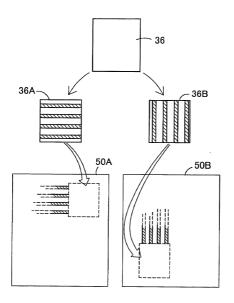
:UPPER METAL WIRING LAYER, WHICH IS PLACED UPWARDLY OVER THE UPPER METAL WIRING LAYER M2 (M3)

FIFTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

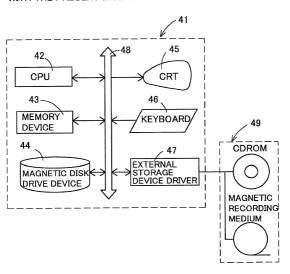




SIXTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNCTIONAL CIRCUIT BLOCKS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED TO FORM A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE



BLOCK DIAGRAM OF A WIRING APPARATUS IN ACCORDANCE WITH THE PRESENT INVENTION



A FLOW CHART OF A WIRING METHOD FOR WIRING IN A FUNCTIONAL CIRCUIT BLOCK USING THE FUNCTIONAL CIRCUIT BLOCKS IN ACCORDANCE WITH THE PRESENT INVENTION

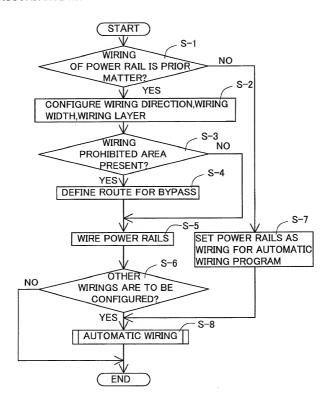
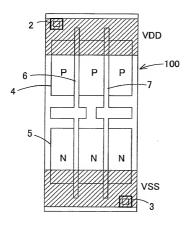


FIG. 12 PRIOR ART

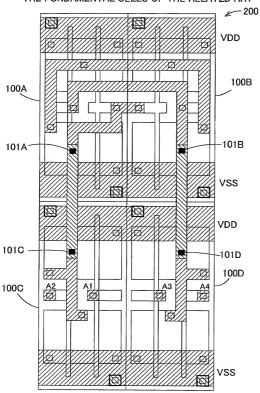
FUNDAMENTAL CELL IN ACCORDANCE WITH THE RELATED ART



:LOWEST METAL WIRING LAYER(M1)

FIG. 13 PRIOR ART

FUNCTIONAL CIRCUIT BLOCK FORMED BY USING THE FUNDAMENTAL CELLS OF THE RELATED ART

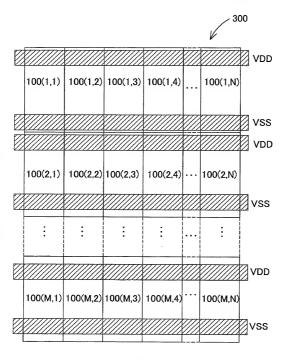


TITISTE TEST

:LOWEST METAL WIRING LAYER(M1)::UPPER METAL WIRING LAYER(M2)

FIG. 14 PRIOR ART

POWER RAIL EMBODIMENT WHEN FORMING THE FUNDAMENTAL CELLS OF THE RELATED ART IN A FORM OF MATRIX



:LOWEST METAL WIRING LAYER(M1)